This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Currently Amended) The method of claim [[1]] 3, wherein after completion of the second pass of self-test, transporting the failing data column and unique failing row addresses to e-fuse macros for permanent storage in the RAM memory.

3. (Currently Amended) A ~~The~~ method ~~of claim 1, wherein determining the worst failing column comprises~~ for self-testing, allocating and repairing a Random Access Memory (RAM) using a spare data column and spare rows comprising:

performing first and second passes of self-test on the RAM memory;

in the first pass of self-test, determining a worst failing data column of the RAM memory by testing one data column at a time while counting the number of unique failing row addresses of the tested data column by masking all data columns except the tested data column, such that only the un-masked tested data column can produce an error in a data-out comparator;

after completion of the first pass of self-test, allocating the spare data column to replace the worst failing data column;

in the second pass of self-test, determining unique failing row addresses in the memory;

after completion of the second pass of self-test, allocating the spare rows to replace the failing rows.

4. (Currently Amended) The method of claim 3, wherein a decoder is used to mask all data columns except the tested data column.

5. (Currently Amended) The method of claim 4, wherein during the first pass of self-test a Built-In Self Test (BIST) generates a data column address signal designating a particular data column in memory to be selected and tested, which is input to said decoder to select the particular data column to be tested, and during normal operation of the RAM a stored worst data column address signal is decoded by decoder to implement the redundant data column in place of the worst tested data column.

6. (Original) The method of claim 3, wherein a pass/fail signal from the data-out comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address.

7. (Currently Amended) The method of claim 3, wherein as each unique failing row address is stored, a counter is enabled to count the number of unique failing row addresses for the unmasked data column, and at the end of testing of the unmasked data column, if the error count value for the unmasked data column exceeds a previously stored high error count value from previously tested data columns, then the unmasked data column is determined to be the worst data column so far, and the error count value for the unmasked data column is stored in an error count register, and a bit-address for

the unmasked data column is stored in a repair register.

8. (Currently Amended) The method of claim 7, wherein after completion of the first pass of self-test, the stored bit-address stored in the repair register is used to enable the spare data column, prior to the second pass of the self-test, and a decoder is used to select steering multiplexers for implementing the spare data column.

9. (Original) The method of claim 6, wherein during the second pass of self-test, the FAR stores unique failing row addresses, and at the end of the second pass of self-test, the FAR values are used to allocate and implement the spare rows.

10. (Currently Amended) The method of claim [[1]] 3, wherein a Built-In Self Test (BIST) generates a data column address signal designating a particular column in memory to be selected and tested, which is input to a first register which, which during BIST column testing, outputs the data column address signal through a multiplexer to a decoder to select the particular data column to be tested, the first register also outputs the worst tested data column address signal to a second repair register, and during normal operation of the RAM the second repair register outputs the stored worst data column address through the multiplexer to said decoder to implement the redundant data column in place of the worst tested data column.

11. (Currently Amended) The method of claim [[1]] 3, wherein during the first pass of self-test, all data columns except a selected tested data column are masked or deselected such that only the un-masked selected data column can produce an error in a data-out

comparator, and a pass/fail signal from the data-out comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address, and a counter is enabled to count the number of unique failing row addresses for the unmasked data column.

12. (Currently Amended) The method of claim 11, wherein at the end of testing of the unmasked data column, if the count value for the unmasked data column exceeds a previously stored worst count value from previously tested data columns, then the unmasked data column is determined to be the worst data column so far, the count value for the unmasked data column is stored in an error count register, and a bit-address for the unmasked data column is stored in a repair register.

13. (Currently Amended) The method of claim 12, wherein after testing of each unmasked data column, the FAR and failing row counter are cleared before testing the next data column, and the stored count value is subsequently compared to a count value for a next data column after testing is completed on the next data column, and at the completion of testing of all data columns, the bit-address of worst data column is stored and saved.

14. (Currently Amended) The method of claim [[1]] 3, wherein in wide RAMs, the RAM is divided into sections of adjacent data columns, with each section having its own redundant data column to replace a worst failing data column in that section, and each section is tested in parallel with other sections of data columns.

15. (Currently Amended) The method of claim [[1]] 3, wherein when the number of unique failing row addresses in two data columns exceeds the number of redundant rows in the RAM, the RAM is designated as unrepairable.

16. (Currently Amended) The method of claim [[1]] 3, performed on an embedded RAM within a microprocessor or logic chip.